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Question Paper Code : 21192

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2014.

Sixth Semester

Electrical and Electronics Engineering

EC 1354 — VLSI DESIGN

(Common to Electronics and Communication Engineering)

(Regulation 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define threshold voltage of a MOS transistor.

2. Why are nMOS devices preferred over pMOS devices?

3. Draw the stick encoding diagram for the n and p diffusion.

4. Draw 2:1 MUX using transmission gate.

5. What are the limitations in fabricating inductance in ICs?

6. What is scaling? Why do we need it?

7. What are the various objectives of placement in the physical design process?

8. List the methods of CMOS testing.

9. List the various types of design styles in verilog HDL.

10. Write an expression to generate and propagate signals in a circuit using verilog HDL.

PART B — (5 × 16 = 80 marks)

11. (a) Draw the small signal model of a MOS transistor and explain its AC characteristics.

Or

(b) (i) Explain the second order effects in MOS device design. (8)

(ii) Explain in detail, n well CMOS fabrication process with necessary diagrams. (8)

12. (a) Explain the operation of inverting and non-inverting super buffer with necessary diagrams. (16)

Or

(b) (i) Draw the stick diagram and layout diagram of a CMOS 2 input-NAND gate. (8)

(ii) Explain the structure and properties of dynamic CMOS logic design. (8)

13. (a) (i) Analyze the CMOS inverter circuit driving the large capacitance loads. (10)

(ii) Write short notes about the transistor sizing for the performance in combinational networks. (6)

Or

(b) Describe in detail about the resistance and capacitance estimation calculation in a CMOS circuit with proper loads and drivers.

14. (a) (i) Design a generic carry look ahead adder. (10)

(ii) Brief on high speed adder circuits. (6)

Or

(b) (i) Design a circuit for a 4 bit unsigned magnitude comparator and explain. (8)

(ii) Describe about delay modeling and clock distribution in ICs. (8)

15. (a) (i) Explain the various data types in verilog HDL. (8)

(ii) Design and model an adder circuit using verilog HDL. Write a test bench. (8)

Or

(b) Explain the various modeling procedures in verilog HDL with suitable examples.